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10/506,497	09/03/2004	Einar Nygard	NYGARD3	1569

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EXAMINER	
LEE, PATRICK J	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/506,497	NYGARD, EINAR	
	Examiner	Art Unit	
	Patrick J. Lee	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-52* is/are rejected.

7)☒ Claim(s) *24,30 and 52* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 September 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0105*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because multiple figures are unclear due to shading of the components in the drawings. For example, in figure 7, the polycrystalline sensor material (37) should have an edge delineated towards the rear. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

4. The drawings are objected to because figure 8 does not seem to correspond to the flipped object of figure 7. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

6. Claims 24, 30, & 52 are objected to because of the following informalities:

With respect to claims 24, 30, & 52, the preambles of the claims are inconsistent with the other similarly dependent claims. To overcome this objection, the elements of the independent claims should be explicitly stated within the dependent claims as to re-write claims 24, 30, & 52 into independent form. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-52 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claims 1-2 & 25-26, the claims state a term "unexposed surface". However, it is indefinite as to which surface this refers to – it could either refer to the unexposed surface of the wafer, or the unexposed surface of the sensor material. As a result, independent claims 1-2 & 25-26 and dependent claims 3-24 & 27-52 are rejected.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-5, 20-27, 29-34, & 48-52 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,510,195 B1 to Chappo et al.

With respect to claim 1, Chappo et al disclose a solid-state detector apparatus comprising: carrier substrate (58) as a wafer, and photodiode array (52) as a sensor material. First, Chappo et al disclose integrating readout electronics (60) onto substrate (58) on a first surface with appropriate contacts and terminal nodes – this corresponds to the method step of integrating electronic processing circuits onto a wafer. Second, Chappo et al also disclose the carrier substrate (58) to provide a conductive path routing the photodiode array (52) to the electronics (60), which would correspond to the step of providing an electrically conductive via through wafer. And finally, Chappo et al disclose the depositing of photodiode array (52, 152, 252) as a sensor material bonded through bumps (56) so that an unexposed surface of the substrate (58) corresponds to each one of the vias.

With respect to claim 2, Chappo et al disclose a solid-state detector apparatus comprising: carrier substrate (58) as a wafer, and photodiode array (52) as a sensor material. First, Chappo et al disclose integrating readout electronics (60) onto substrate (58) on a first surface with appropriate contacts and terminal nodes – this corresponds to the method step of integrating electronic processing circuits onto a wafer. Second, Chappo et al also disclose the carrier substrate (58) to provide a conductive path routing the photodiode array (52) to the electronics (60), which would correspond to the step of providing an electrically conductive via through wafer. And finally, Chappo et al disclose the depositing of photodiode array (52, 152, 252) as a sensor material bonded

through bumps (56) so that an unexposed surface of the substrate (58) corresponds to each one of the vias.

With respect to claim 3, Chappo et al inherently disclose the plurality of bond pads on wafer attached to bumps (56) as a plurality of metallized terminal pads.

With respect to claim 4, Chappo et al illustrate using multiple arrays to divide the integrated circuit into discrete sensor arrays (see figure 2B).

With respect to claim 5, Chappo et al illustrate assembling multiple arrays edge to edge to form a composite sensor array with an extended surface area (see figure 2B).

With respect to claim 20, Chappo et al illustrate the scribing of lines to produce individual sensor chips (see figure 2B).

With respect to claim 21, Chappo et al inherently disclose the plurality of bond pads on wafer attached to bumps (56) as a plurality of metallized terminal pads.

With respect to claim 22, Chappo et al illustrate assembling multiple arrays edge to edge to form a composite sensor array with an extended surface area (see figure 2B).

With respect to claim 23, Chappo et al disclose this device to be for an X-radiation detector as a high-energy photon-imaging detector.

With respect to claim 24, Chappo et al disclose the device in a sensor array or module.

With respect to claim 25, Chappo et al disclose a solid-state detector apparatus comprising: carrier substrate (58) as a wafer with integrating readout electronics (60)

onto substrate (58) on a first surface with appropriate contacts and terminal nodes; and photodiode array (52) as a sensor material. Chappo et al also disclose the carrier substrate (58) to provide a conductive path routing the photodiode array (52) to the electronics (60), which would correspond to the step of providing an electrically conductive via through wafer. Also, Chappo et al disclose the depositing of photodiode array (52, 152, 252) as a sensor material bonded through bumps (56) so that an unexposed surface of the substrate (58) corresponds to each one of the vias.

With respect to claim 26, Chappo et al disclose a solid-state detector apparatus comprising: carrier substrate (58) as a wafer with integrating readout electronics (60) onto substrate (58) on a first surface with appropriate contacts and terminal nodes; and photodiode array (52) as a sensor material. Chappo et al also disclose the carrier substrate (58) to provide a conductive path routing the photodiode array (52) to the electronics (60), which would correspond to the step of providing an electrically conductive via through wafer. Also, Chappo et al disclose the depositing of photodiode array (52, 152, 252) as a sensor material bonded through bumps (56) so that an unexposed surface of the substrate (58) corresponds to each one of the vias.

With respect to claim 27, Chappo et al disclose this device to be for an X-radiation detector as a high-energy photon-imaging detector.

With respect to claim 29, Chappo et al inherently disclose the plurality of bond pads on wafer attached to bumps (56) as a plurality of metallized terminal pads.

With respect to claim 30, Chappo et al illustrate assembling multiple arrays edge to edge to form a composite sensor array with an extended surface area (see figure 2B).

With respect to claim 31, exposed surface of photodiode array (52) forms a first electrode to which incident photons are directed, while bottom of the surface of photodiode array (52) has contact pads (54) as multiple second electrodes corresponding to vias on substrate (58) through bumps (56).

With respect to claim 32, Chappo et al inherently disclose the plurality of bond pads on wafer attached to bumps (56) as a plurality of metallized terminal pads.

With respect to claim 33, Chappo et al illustrate using multiple arrays to divide the integrated circuit into discrete sensor arrays (see figure 2B).

With respect to claim 34, Chappo et al illustrate assembling multiple arrays edge to edge to form a composite sensor array with an extended surface area (see figure 2B).

With respect to claim 48, Chappo et al illustrate the scribing of lines to produce individual sensor chips (see figure 2B).

With respect to claim 49, Chappo et al inherently disclose the plurality of bond pads on wafer attached to bumps (56) as a plurality of metallized terminal pads.

With respect to claim 50, Chappo et al illustrate assembling multiple arrays edge to edge to form a composite sensor array with an extended surface area (see figure 2B).

With respect to claim 51, Chappo et al disclose this device to be for an X-radiation detector as a high-energy photon-imaging detector.

With respect to claim 52, Chappo et al disclose the device in a sensor array or module.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 6-19, 28, & 35-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,510,195 B1 to Chappo et al.

Chappo et al disclose the device as described in the discussion of claims 1-5, 20-27, 29-34, & 48-52.

With respect to claim 6, Chappo et al does not explicitly disclose the thinning down of the wafer, but such would have been obvious to one of ordinary skill in the art because such would reduce the size of the device and the amount of materials needed to construct the device.

With respect to claim 7, the modified Chappo et al does not explicitly disclose pre-thinning the wafer, but such would have been obvious to one of ordinary skill in the art in order to prevent the wasting of resources in producing the device.

With respect to claim 8, the modified Chappo et al disclose the substrate (58) to be a printed circuit substrate carrying metal tracings. However, the modified Chappo et

al does not explicitly disclose the coating of the first surface with a photomask and implanting the wafer with impervious material. Such would have been obvious to one of ordinary skill in the art because such would allow for accurate creation of the vias for proper alignment between the photodiode array and the integrated circuits.

With respect to claim 9, the modified Chappo et al disclose the substrate (58) to be a printed circuit substrate carrying metal tracings. However, the modified Chappo et al does not explicitly disclose the producing of a complementary photomask on the first surface of the wafer. Such would have been obvious to one of ordinary skill in the art because such would allow for accurate creation of the vias for proper alignment between the photodiode array and the integrated circuits.

With respect to claim 10, the modified Chappo et al imply the different materials for the substrate (see column 7, lines 25-31), but do not explicitly state that the substrate is based on silicon. However, such would have been obvious to one of ordinary skill in the art because silicon is an inexpensive material widely used in the manufacture of substrates.

With respect to claim 11, the modified Chappo et al does not explicitly disclose the etching of holes through the substrate (58) with a photomask, but does disclose the formation of vias, so that contacts (57, 70) are placed through the substrate (58). However, such would have been obvious to one of ordinary skill in the art because such would allow for accurate marking and formation of the vias.

With respect to claims 12-14, the modified Chappo et al disclose the substrate (58) to be a printed circuit substrate carrying metal tracings. However, the modified

Chappo et al does not explicitly disclose the coating of the first surface with a photomask and implanting the wafer with impervious material. Such would have been obvious to one of ordinary skill in the art because such would allow for accurate creation of the vias for proper alignment between the photodiode array and the integrated circuits.

With respect to claims 15-16, the modified Chappo et al does not explicitly disclose the etching of holes through the substrate (58) with a photomask, but does disclose the formation of vias, so that contacts (57, 70) are placed through the substrate (58). However, such would have been obvious to one of ordinary skill in the art because such would allow for accurate marking and formation of the vias.

With respect to claims 17-18, the modified Chappo et al does not explicitly disclose the growth of amorphous or polycrystalline sensor material, but such would have been obvious to one of ordinary skill in the art in order to obtain the absorptive capabilities to capture high-energy photons.

With respect to claim 19, the modified Chappo et al does not explicitly disclose pre-thinning the wafer, but such would have been obvious to one of ordinary skill in the art in order to prevent the wasting of resources in producing the device.

With respect to claim 35, Chappo et al does not explicitly disclose the thinning down of the wafer, but such would have been obvious to one of ordinary skill in the art because such would reduce the size of the device and the amount of materials needed to construct the device.

With respect to claim 36, the modified Chappo et al does not explicitly disclose pre-thinning the wafer, but such would have been obvious to one of ordinary skill in the art in order to prevent the wasting of resources in producing the device.

With respect to claim 37, the modified Chappo et al disclose the substrate (58) to be a printed circuit substrate carrying metal tracings. However, the modified Chappo et al does not explicitly disclose the coating of the first surface with a photomask and implanting the wafer with impervious material. Such would have been obvious to one of ordinary skill in the art because such would allow for accurate creation of the vias for proper alignment between the photodiode array and the integrated circuits.

With respect to claim 38, the modified Chappo et al disclose the substrate (58) to be a printed circuit substrate carrying metal tracings. However, the modified Chappo et al does not explicitly disclose the producing of a complementary photomask on the first surface of the wafer. Such would have been obvious to one of ordinary skill in the art because such would allow for accurate creation of the vias for proper alignment between the photodiode array and the integrated circuits.

With respect to claim 39, the modified Chappo et al imply the different materials for the substrate (see column 7, lines 25-31), but do not explicitly state that the substrate is based on silicon. However, such would have been obvious to one of ordinary skill in the art because silicon is an inexpensive material widely used in the manufacture of substrates.

With respect to claim 40, the modified Chappo et al does not explicitly disclose the etching of holes through the substrate (58) with a photomask, but does disclose the

formation of vias, so that contacts (57, 70) are placed through the substrate (58). However, such would have been obvious to one of ordinary skill in the art because such would allow for accurate marking and formation of the vias.

With respect to claims 41-43, the modified Chappo et al disclose the substrate (58) to be a printed circuit substrate carrying metal tracings. However, the modified Chappo et al does not explicitly disclose the coating of the first surface with a photomask and implanting the wafer with impervious material. Such would have been obvious to one of ordinary skill in the art because such would allow for accurate creation of the vias for proper alignment between the photodiode array and the integrated circuits.

With respect to claims 44-45, the modified Chappo et al does not explicitly disclose the etching of holes through the substrate (58) with a photomask, but does disclose the formation of vias, so that contacts (57, 70) are placed through the substrate (58). However, such would have been obvious to one of ordinary skill in the art because such would allow for accurate marking and formation of the vias.

With respect to claim 47, the prior formation of the sensor material and the terminal connections before the formation of the processing circuits is not explicitly disclosed, but such would have been obvious to one of ordinary skill in the art in order to allow for appropriate assembly of the elements.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 5,734,201 to Djennas et al and US 6,091,070 to Linngren et al disclose semiconductive devices.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick J. Lee whose telephone number is (571) 272-2440. The examiner can normally be reached on Monday through Friday, 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on (571) 272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Patrick J. Lee
Examiner
Art Unit 2878

PJL
March 10, 2006

Stephone B. Allen
Primary Examiner